CLAIMS

Sub A1

1. An apparatus comprising:

a first circuit configured to present a parallel output data in response to (i) a first clock signal and (ii) one or more serial data signals; and

a second circuit configured to present said one or more serial data signals and said first clock signal in response to (i) a second clock signal and (ii) a parallel input data signal.

2. The apparatus according to claim 1, wherein said first clock signal comprises a bit clock signal.

3. The apparatus according to claim 1, wherein said second clock signal comprises a reference clock signal.

4. The apparatus according to claim 1, wherein said first circuit further comprises:

a third circuit configured to generate (i) one or more select signals and (ii) a selected clock signal in response to (i) said first clock signal and (ii) a phase select signal.

5. The apparatus according to claim 4, wherein said first circuit further comprises:

a phase comparator circuit configured to generate said phase select signal in response to said one or more select signals and one of said one or more serial data signals.

6. The apparatus according to claim 4, wherein said third circuit comprises a phase generation and select circuit.

7. The apparatus according to claim 4, wherein said first circuit includes a deserializer circuit configured to generate said parallel output data signal in response to said selected clock signal and another one of said one or more serial data signals.

8. The apparatus according to claim 7, wherein said first circuit further comprises:

a multiplexer configured to generate (i) said one of said one or more serial data signals and (ii) said another one of said one or more serial data signals, in response to said one or more serial data signals.

9. A circuit comprising:

means for generating a parallel output data in response to (i) a first clock signal and (ii) one or more serial data signals; and

means for generating said one or more serial data signals and said first clock signal in response to (i) a second clock signal and (ii) a parallel input data signal.

10. A method for controlling a pulse width in a phase and/or frequency detector comprising the steps of:

(A) generating a parallel output data in response to (i) a first clock signal and (ii) one or more serial data signals; and

(B) generating said one or more serial data signals and said first clock signal in response to (i) a second clock signal and (ii) a parallel input data signal, wherein said first clock signal is configured to control said pulse width.

11. The method according to claim 10, wherein said first clock signal comprises a bit clock signal.

12. The method according to claim 10, wherein said second clock signal comprises a reference clock signal.

13. The method according to claim 10, wherein step (A) further comprises the sub-step of:

generating (i) one or more select signals and (ii) a selected clock signal in response to (i) said first clock signal and (ii) a phase select signal.

14. The method according to claim 13, wherein step (A) further comprises the sub-step of:

generating said phase select signal in response to said one or more select signals and one of said one or more serial data signals.

15. The method according to claim 14, wherein step (A) further comprises the sub-step of:

generating said parallel output data signal in response to said selected clock signal and another one of said one or more serial data signals.

16. The method according to claim 15, further comprising the step of:

generating said one of said one or more serial data signals and said another one of said one or more serial data signals, in response to said one or more serial data signals.

Add A3

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